

PY32E407V1xT-START-ETH V2

User Guide



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1. Introduction

The PY32E407V1xT-START-ETH V2 development board integrates a PY-LINK emulator. For detailed usage instructions of PY-LINK, please refer to the document "PY-Link OB_UserManual_EN.pdf". The START board uses the PY32E407V1xT as the main controller. This development board, equipped with a 32-bit ARM® Cortex®-M4F CPU core from Puya, provides a simple hardware development environment. The board is powered via the USB interface of PY-LINK. It offers peripheral resources including extension pins, as well as USB、ETH、SWD, Reset, Boot, User button key, Reset key, LED, and more. This document provides detailed hardware schematics and related application examples.

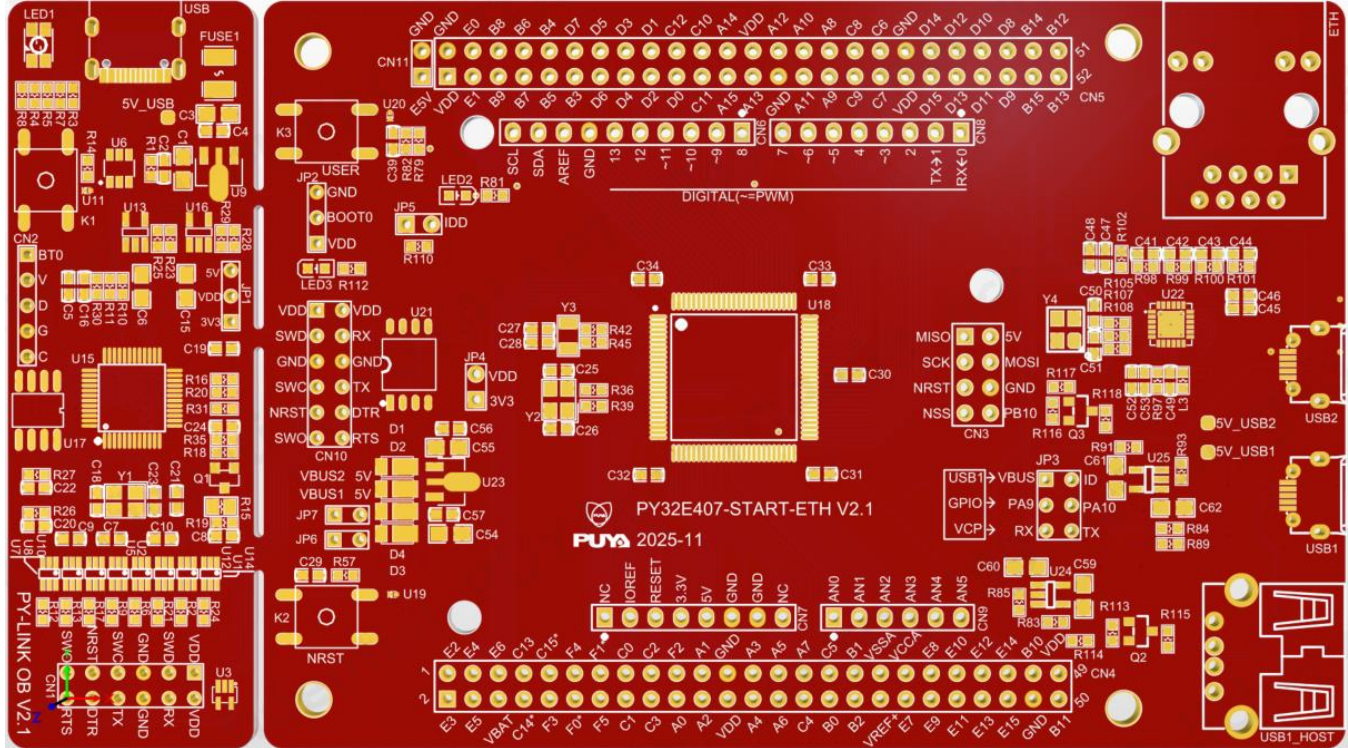


Figure 1-1 PCB 3D renderings

2. Functional pin assignment

Table 2-1 Pin Assignment

Function	Pin	Description	Note
LED	\	LED1	PY-LINK LED
	\	LED2	VDD*
	PB5	LED3	User LED
KEY	\	K1	PY-LINK Key
	PB6	K2	User Key
	PF5	K3	Reset Key
SPI	PA4	SPI_NSS	ExternalFLASH
	PB3	SPI_CLK	ExternalFLASH
	PA6	SPI_MISO	ExternalFLASH
	PA7	SPI_MOSI	ExternalFLASH
ESMC	PD2	ESMC_CS	ExternalFLASH
	PA3	ESMC_SCK	ExternalFLASH
	PB1	ESMC_IO0	ExternalFLASH
	PB0	ESMC_IO1	ExternalFLASH
	PA7	ESMC_IO2	ExternalFLASH
	PA6	ESMC_IO3	ExternalFLASH

3. Overview of Hardware Design

The development board is powered via a Type-C USB connection. To download programs to the board, a Type-C USB cable is required. Select the correct boot mode, connect the USB cable, and if LED1 lights up, it indicates a proper power connection.

3.1 Power Supply

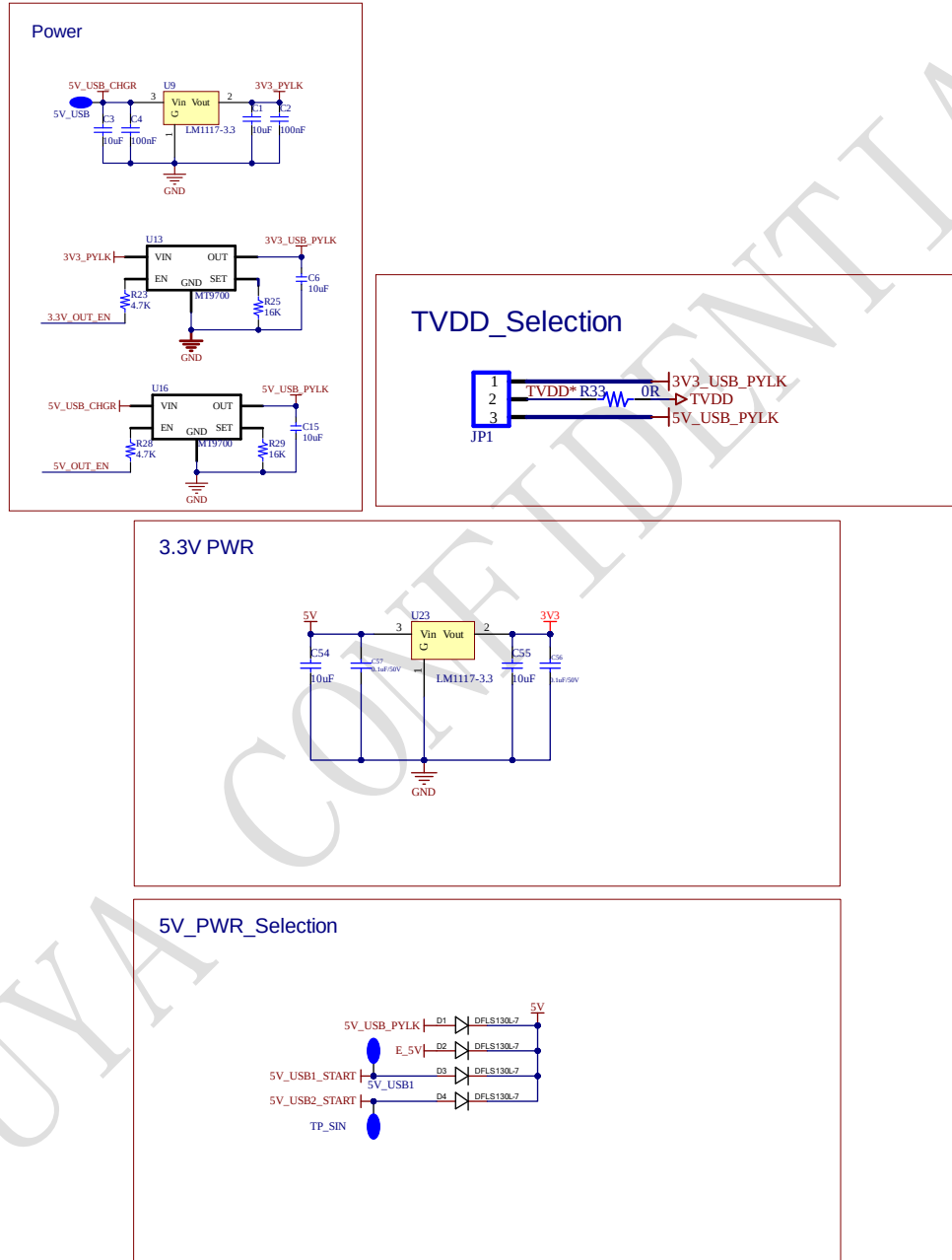


Figure 3-1 Power Supply Schematic

3.2 I_{DD} TEST

When JP5 OFF (symbol IDD) and R110 OFF, an ammeter can be connected to measure the power consumption of MCU.

JP5 OFF, R110 ON:MCU is powered. (Default setting and JP5 plug is not mounted before shipping)

JP5 ON, R110 OFF:MCU is powered.

JP5 OFF, R110 OFF:An ammeter must be connected. If there is no ammeter available, the MCU cannot be powered.

VDD_Selection

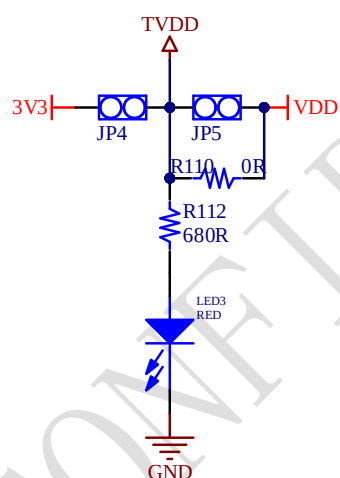


Figure 3-2 I_{DD} Schematic

3.3 LED Indicator Light

The red LED indicates that the board TVDD is powered as shown in the figure above; The green LED is the user LED connected to the PB5 (default) pin or PC10 pin of the MCU.

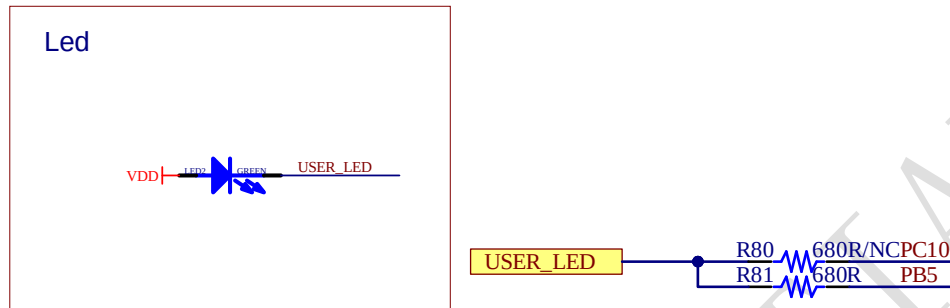


Figure 3-3 LED Schematic

3.4 Reset Key

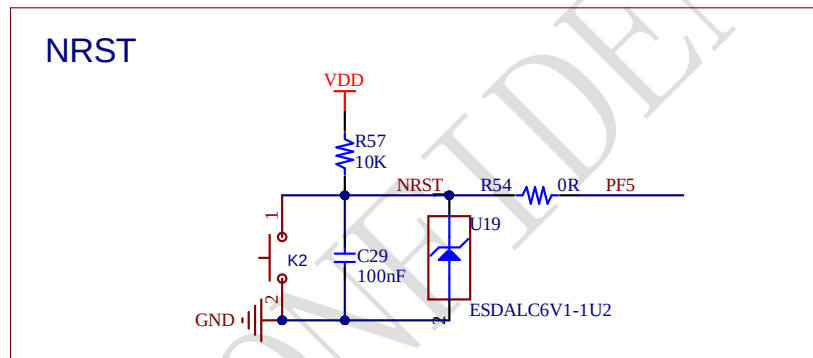


Figure 3-4 Reset Key Schematic

3.5 User Key

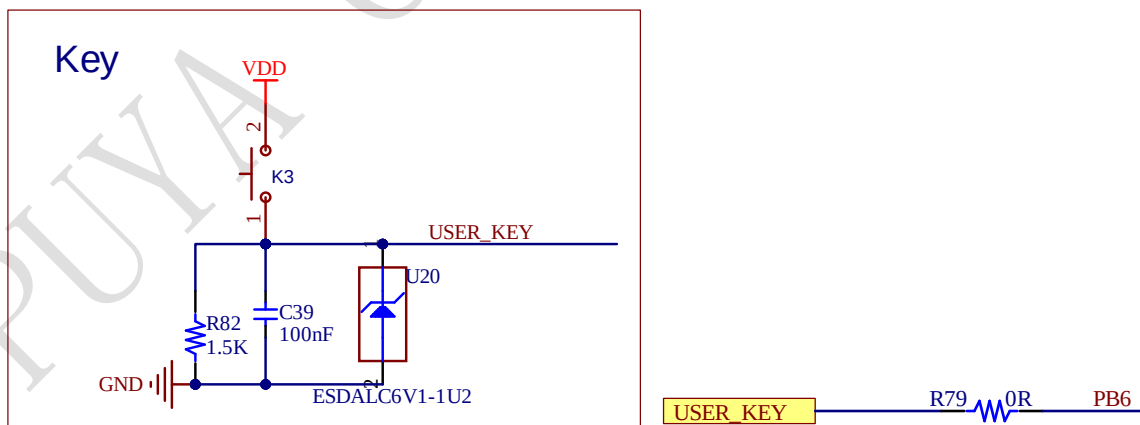


Figure 3-5 User Key Schematic

3.6 Boot Mode Selection

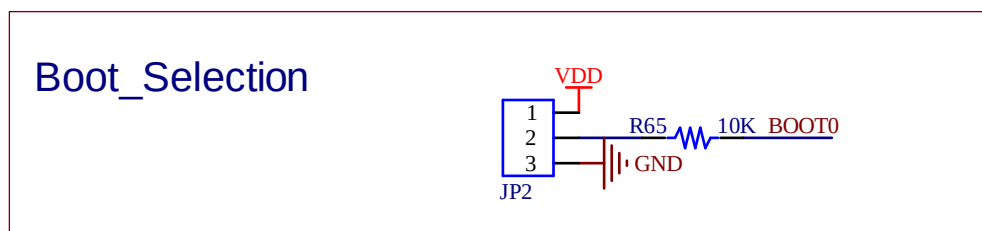


Figure 3-5 BOOT Mode Schematic

By configuring the BOOT0 Pin, nBOOT0 / nBOOT1 / nSWBOOT0 (stored in Option bytes), you can choose from three different boot modes, as shown in the following table:

Table 3-6 Boot configuration

Boot mode configuration					Mode
BOOT_LOCK	nBOOT1 FLASH_OPTR2[8]	nBOOT0 FLASH_OPTR2[14]	BOOT0 Pin PB8	nSWBOOT0 FLASH_OPTR2[13]	
1	X	X	X	X	Main Flash memory is selected as the boot area
0	X	X	0	1	Main Flash memory is selected as the boot area
0	X	1	X	0	Main Flash memory is selected as the boot area
0	0	X	1	1	Embedded SRAM1 is selected as the boot area
0	0	0	X	0	Embedded SRAM1 is selected as the boot area
0	1	X	1	1	System memory is selected as the boot area
0	1	0	X	0	System memory is selected as the boot area

3.7 External Clock Source

HSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 24 MHz crystal is used as HSE clock source.

Oscillator from external PF0:

External oscillator is injected from the PF0 of CN4. The hardware must be configured: R36 OFF.

HSE unused

MCU PF0 and PF1 are used as GPIOs.

LSE clock source

There are three methods to configure the external low-speed clock sources by hardware:

On-board crystal (Factory default setting):

On-board 32.768 kHz crystal is used as HSE clock source.

Oscillator from external PC14:

External oscillator is injected from the PC14 of CN4. The hardware must be configured: R42 OFF.

LSE unused

MCU PC14 and PC15 are used as GPIOs.

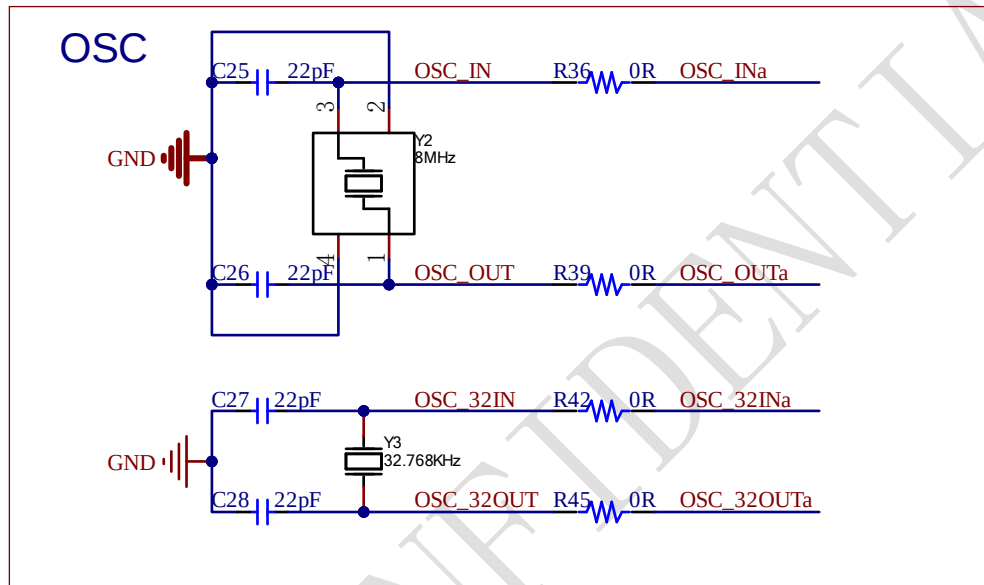


Figure 3-8 Clock source function schematic

3.8 Programming and debugging:

The evaluation board integrates PY-LINK for users to program/debug the PY32E407V1xT on the PY32E407V1xT-START-ETH V2 board. PY-LINK supports SWD interface mode, and supports a set of virtual serial ports (VCP) and PY32E407V1xT's USART1_TX/USART1_RX (PA9/PA10) to connect and communicate through Dupont wire, please refer <USART> to the official PY32xxxx_Firmware Example. For more information about PY-LINK operation, firmware upgrade, and precautions, please refer to the "PY-LINK OB_UserManual_EN.pdf" document. The PY-LINK on board can be disassembled or separated from the PY32E407V1xT-START-ETH V2. In this case, the PY32E407V1xT-START-ETH V2 can still be connected to the CN1 interface (not mounted before leaving factory) of PY-LINK through CN10 interface (not mounted before leaving factory), or to another PY-LINK, in order to continue to program and debug the PY32E407V1xT.

4. Guide to Using the Example

4.1 LED Example

Purpose of the Example

There is one LED on the development board, the LED is controlled by GPIO. This sample program will tell how to light up the LED.

Execution Results

Download the official PY32xxxx_Firmware Example <GPIO_Toggle> to the board, reset and run, and the green LED flashes.

4.2 KEY Example

Purpose of the Example

There is 1 user button on the board. The user key is detected by the GPIO. This routine will show you how to detect a key with an external interrupt.

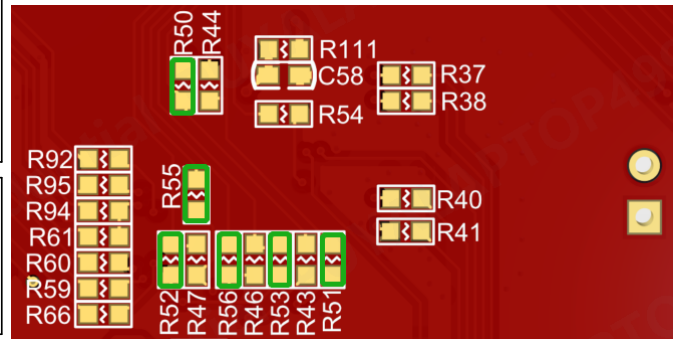
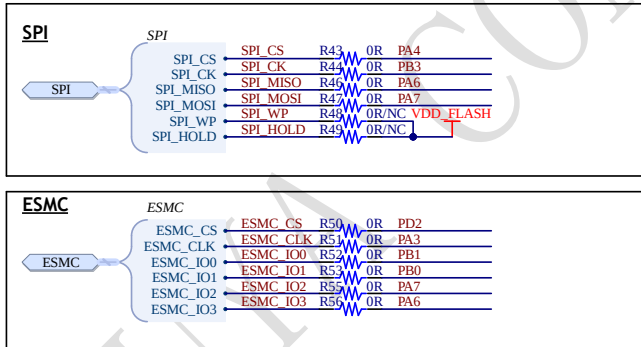
Execution Results

Download the official PY32xxxx_Firmware Example <EXTI_IT> to the board, reset and run, press the button once, and the green LED will switch to the on-off state once.

4.3 FLASH Example

Purpose of the ESMC Example

There is only one FLASH on the development board, and only one communication mode can be selected between ESMC and SPI, and ESMC mode is selected by default. If it has been modified, it is necessary to weld the 0R resistors at the R50, R51, R52, R53, R55 and R56 positions, and not the 0R resistors at the R43, R44, R46, R47, R48, and R49 positions. The specific locations are as follows.

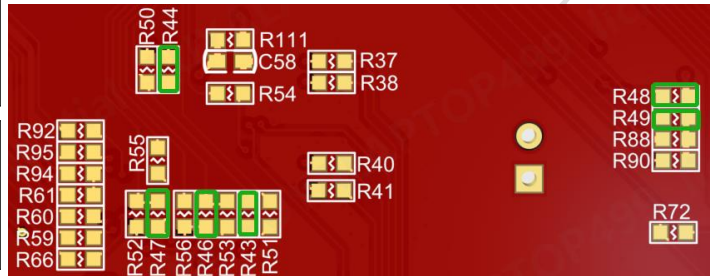
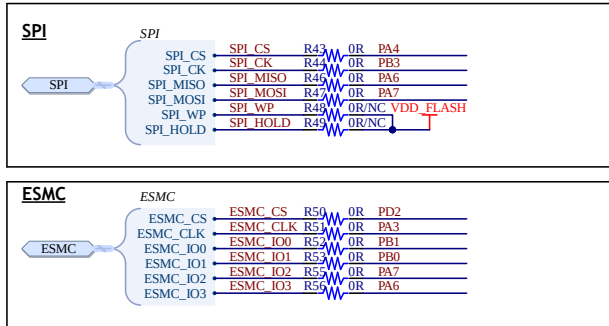


Execution Results

Download the official PY32xxxx_Firmware Example <ESMC_ReadWrite_QSPI_Polling> to the board, reset and run, If the green LED is always on, the FLASH read and write is successful, otherwise the FLASH read and write fails.

Purpose of the SPI Example

There is only one FLASH on the development board, and only one communication mode can be selected between ESMC and SPI, and ESMC mode is selected by default. To change to SPI, you need to remove the 0R resistors at the R50, R51, R52, R53, R55, and R56 positions. Solder 0R resistors at R43, R44, R46, R47, R48, R49 positions. The specific locations are as follows.



Execution Results

Download the official PY32xxxx_Firmware Example< SPI_FullDuplex_ExternalFLASH>to the board, reset and run, If the green LED is always on, the FLASH read and write is successful, otherwise the FLASH read and write fails.

4.4 ETH Example

Purpose of the Example

There is one LAN8720A-CP-TR chip on the development board, which is connected to the chip's Ethernet peripheral module to implement Ethernet communication, and only supports RMII mode. This routine will show you how to communicate over a network.

Execution Results

Download the <TcpEcho_RMII>official PY32xxxx_Firmware routine to the development board, connect the network cable to the development board and then connect to the computer, connect the PC10 (TX) to the RX of CN1 and the TX of PC11 (RX) with a Dupont cable, open the serial port debugging assistant, set the computer IP address (you need to set the same network address as the development board), and then open another serial port debugging assistant and connect it with TCPClient. The board is reset to run, press the button once, click the remote connection, enter the content to be sent, and click send to receive the content to be sent.

The serial output is as follows:

```
The local port number is: 5001

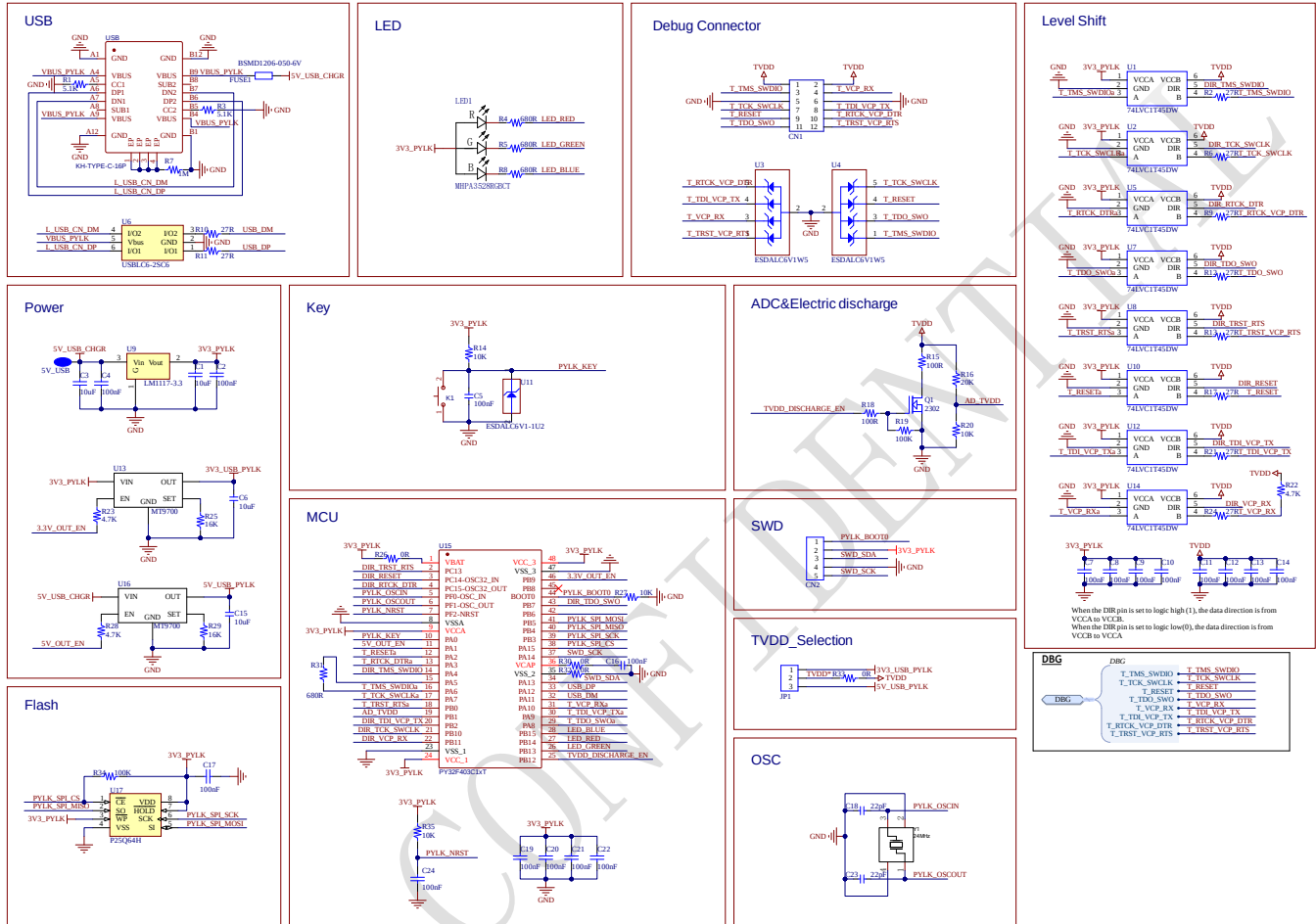
[DEBUG] >> eth hardware init success...The local IP address is: 192.168.0.122
eth receive success
```

The network debug output is as follows:

```
[14:48:58.401]发->◇12345678□
[14:49:01.432]收<-◆12345678
[14:49:03.322]发->◇12345678□
[14:49:06.103]收<-◆12345678
```

5. Schematic

5.1 PY-LINK Schematic



5.2 MCU Schematic

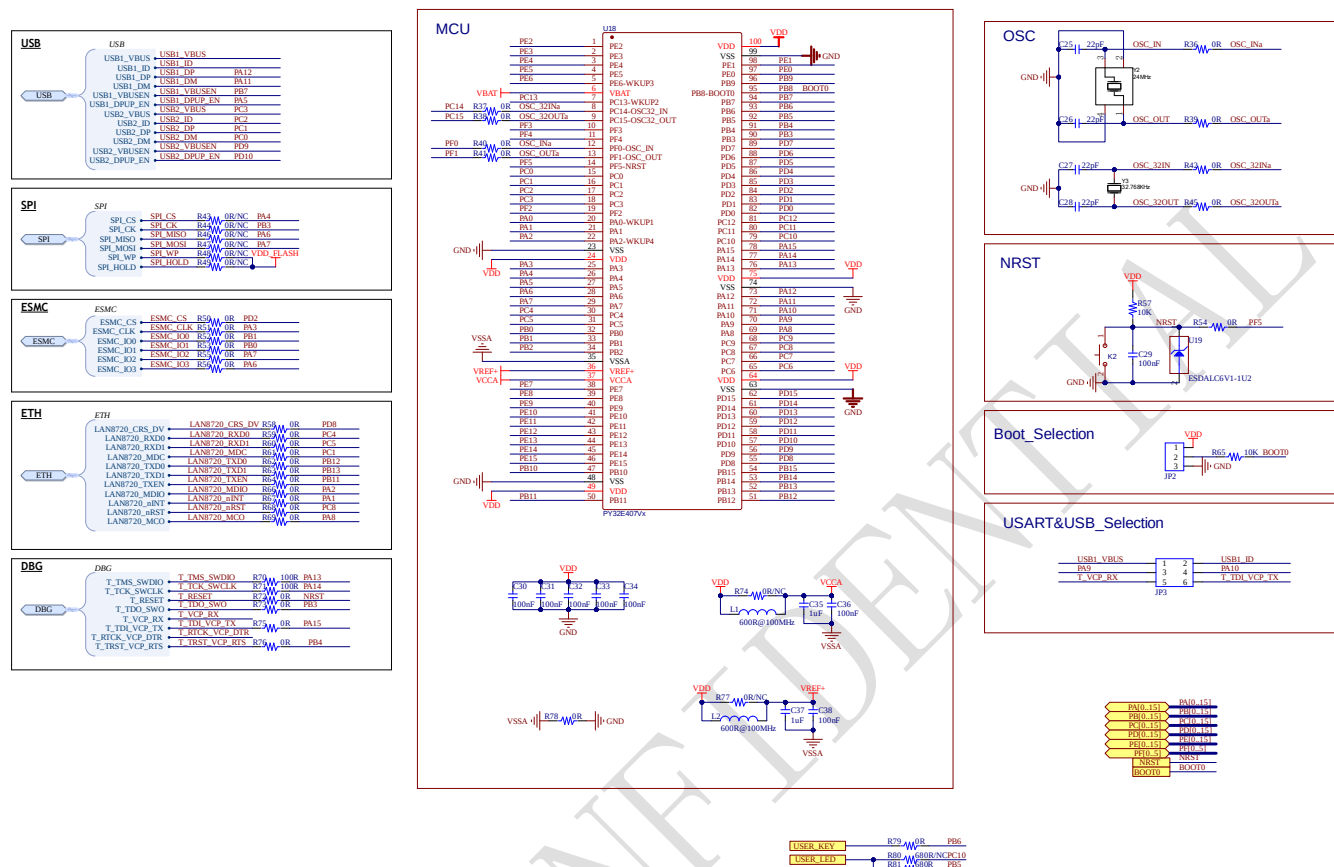
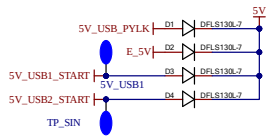


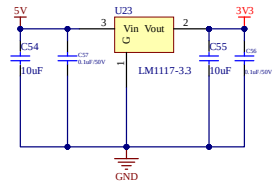
Figure 5-2 MCU Schematic

5.3 POWER Schematic

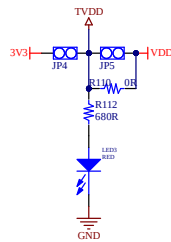
5V_PWR_Selection



3.3V PWR



VDD_Selection



Battery

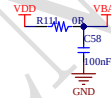


Figure 5-3 POWER Schematic

5.4 ETH Schematic

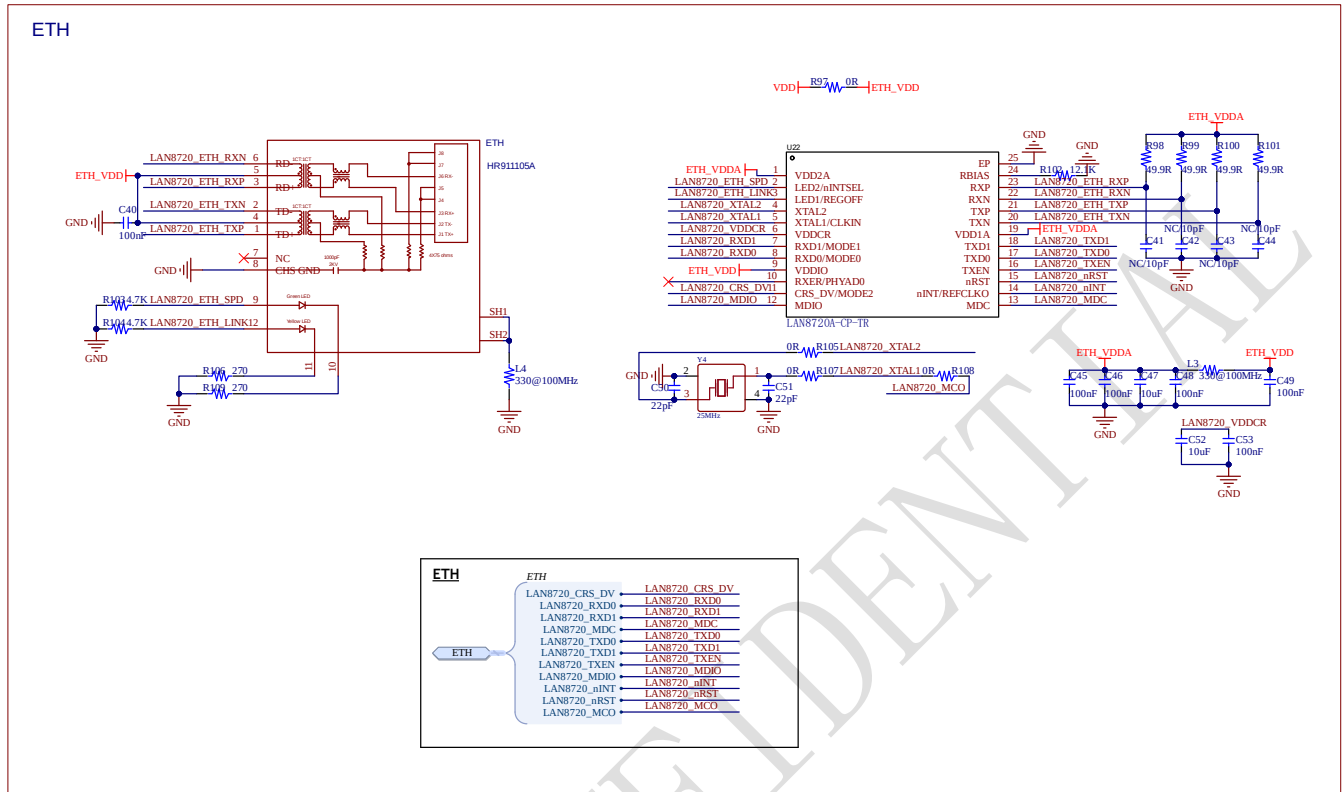


Figure 5-4 POWER Schematic

5.5 External interfaces Schematic

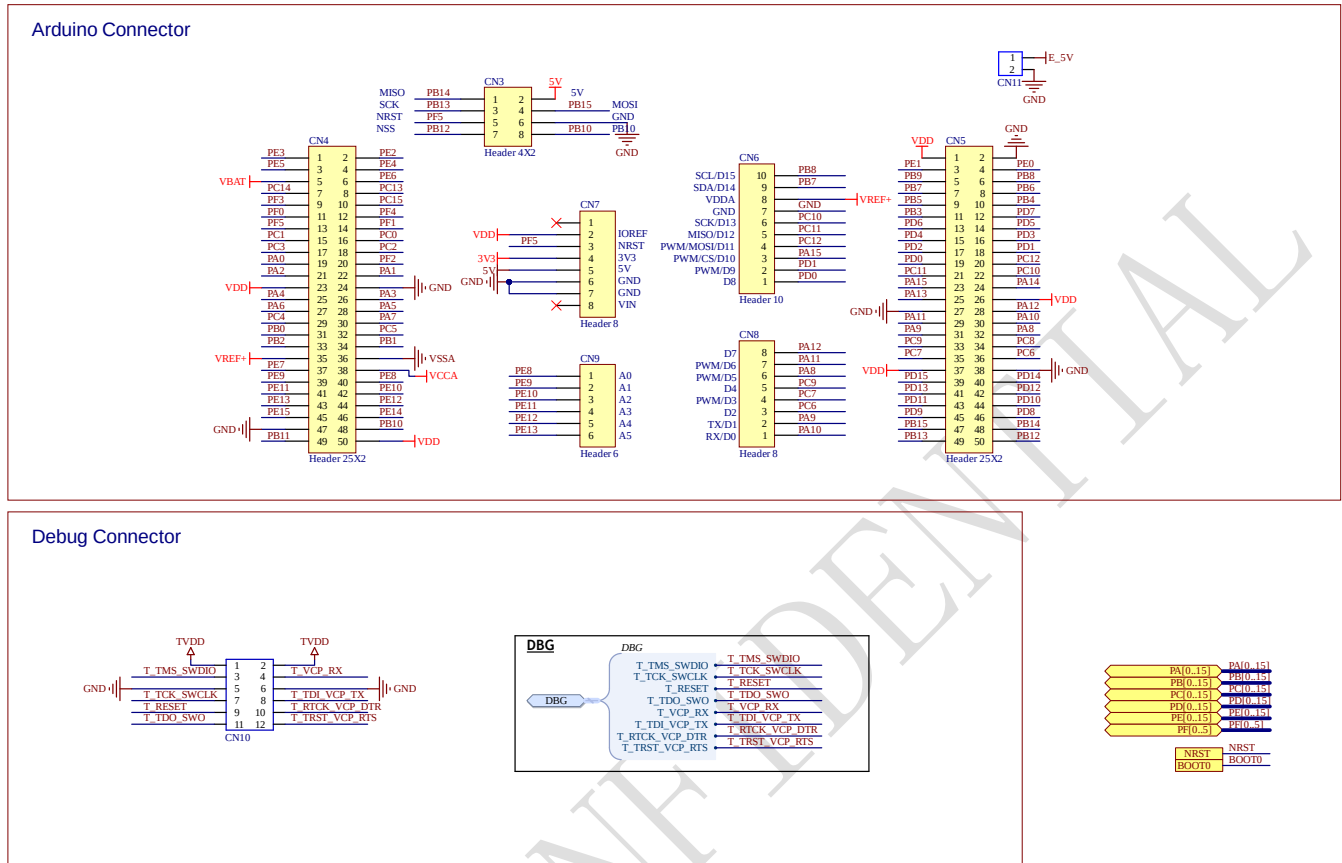


Figure 5-5 External interfaces Schematic

6. Updated History

Version	Content	Date
V1.0	Initial version	2025/07/09
V1.1	Update PYLink&USB&MCU schematic	2025/11/14



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